Fitted Elmore Delay: A Simple and Accurate Interconnect Delay Model *

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ABSTRACT

In this paper, we present a new interconnect delay model called *Fitted Elmore delay* (FED). FED is generated by approximating Hspice delay data using a curve fitting technique. The functional form used in curve fitting is derived based on the Elmore delay model. Thus our model has all the advantages of the Elmore delay model. It has a closed form expression as simple as the Elmore delay model and is extremely efficient to compute. Interconnect optimization with respect to design parameters can also be done as easily as in the Elmore delay model. In fact, most previous algorithms and programs based on Elmore delay model can use our model without much change. Most importantly, FED is significantly more accurate than the Elmore delay model. The maximum error in delay estimation is at most 2% for our model, compared to 8.5% for the scaled Elmore delay model. The average error is less than 0.8%. We also show that FED can be more than 10 times more accurate than Elmore delay model when applied to wire sizing.

1. INTRODUCTION

As the physical dimensions in VLSI technologies scale down, interconnect delay increasingly dominates gate delay in determining circuit performance[1]. As a result, high-level synthesis, logic synthesis, and physical layout tools are becoming more interconnect-centric. In order to take the impact of interconnect delay into account, it is very important to have computationally inexpensive and accurate interconnect delay models.

In the past, many interconnect delay models have been proposed by analyzing the moments of the impulse response [2]. Asymptotic waveform evaluation (AWE) [3] is a generalized approach to response approximation by moment matching. It is very accurate but computationally very expensive. Hence, many moment-matching variants using the first two to four moments have been proposed [4, 5, 6, 7, 8, 9]. Those variants are relatively much more efficient but less accurate. Nevertheless, they may still be too expensive to be used within the tight optimization loops of design synthesis and layout tools. Moreover, for all the models above, the delay is either computed by an iterative procedure or expressed as a sophisticated implicit function of the design parameters. Sensitivity information cannot be easily calculated. Therefore, these models provide little insight into determining the design parameters during design or optimization.

As a result, the Elmore delay (ED) [10], which is the first moment of the impulse response, is the most widely used interconnect delay model during design synthesis and layout[11]. It can be written as a simple, closed form expression in terms of design parameters. It is extremely efficient to compute and it provides useful insight for op-

timization algorithms. It has also been shown to have good fidelity with respect to Hspice simulation [12, 13, 14]. The primary disadvantage of the Elmore delay model is that it has limited accuracy. It always overestimates the delay [15]. So a commonly used variant is to scale the Elmore delay by $\ln 2$ [2]. We call this the scaled Elmore delay (SED). However, it was observed that SED can significantly underestimate a large portion of delays.

In this paper, we propose a new model called *Fitted Elmore delay* (FED). Let r be the sheet resistance, c_a be the unit area capacitance and c_f be the unit fringing capacitance. For an interconnect wire of length l and width w connecting a driver with driver resistance r_d and a load with load capacitance c_l, the Fitted Elmore delay is given by:

$$
\begin{aligned}
FED&(r_d, c_l, l, w) \\
=\ & A \cdot r_d c_a l w + B \cdot r_d c_f l + C \cdot r_d c_l \\
+\ & D \cdot \frac{r c_a l^2}{2} + E \cdot \frac{r c_f l^2}{2w} + F \cdot \frac{r l c_l}{w}
\end{aligned} \tag{1}
$$

The coefficients A, B, C, D, E, and F are determined by a curve fitting technique to approximate Hspice simulation data. The functional form (1) used in fitting the Hspice data is derived based on the Elmore delay model. Although Elmore delay model is not very accurate by itself, it provides useful insight into the dependence of interconnect delay with various parameters. This insight is used by our model.

FED is as simple and as efficient to compute as the Elmore delay model. However, it is significantly more accurate than both ED and SED. The maximum error is only 2% for our model, compared to around 8.5% for the scaled Elmore delay model. Since it is written as a simple analytical expression, optimization of delay with respect to design parameters can be done easily. In fact, because of its striking similarity to Elmore delay model, most interconnect optimization algorithms based on Elmore delay can use our model without much change.

The remainder of the paper is organized as follows: In Section 2, we present the Fitted Elmore delay model for a single wire. We also present some experimental results to show that FED is 4 to 7 times more accurate than SED in delay estimation. In Section 3, we show that FED can be more than 10 times more accurate when applied to wire sizing. In Section 4, we generalize the Fitted Elmore model to handle interconnect trees. In Section 5, we present a *Transformed Elmore delay* (TED) model which has basically the same form as the Elmore delay model, but almost as accurate as FED. In Section 6, we discuss future research directions.

2. FITTED ELMORE DELAY

In this section, we present the derivation and some experimental results for Fitted Elmore delay model on a uniform width wire. The extension to consider interconnect trees is presented in Section 4.

The basic idea is to approximate accurate delay data by curve fitting to an equation. In order to have a simple closed form model, the functional form used in curve fitting is derived based on the Elmore delay model. Although Elmore delay model is not very accurate by itself, it provides useful insight into the dependence of interconnect delay with various parameters.

The notations of technology parameters are listed below.

- W_{min} : the minimum wire width

- r_g: the output resistance of a minimum device

- c_g: the input capacitance of a minimum device

- r: the sheet resistance

- c_a: the unit area capacitance

- c_f: the unit fringing capacitance

For an interconnect wire of length l and width w connecting a driver with driver resistance r_d and a load with load capacitance c_l, the Elmore delay is given by:

$$
\begin{aligned}
&ED(r_d, c_l, l, w) \\
&= r_d(c_a l w + c_f l + c_l) + \frac{rl}{w}\left(\frac{c_a l w}{2} + \frac{c_f l}{2} + c_l\right) \quad (2) \\
&= r_d c_a l w + r_d c_f l + r_d c_l + \frac{r c_a l^2}{2} + \frac{r c_f l^2}{2w} + \frac{r l c_l}{w} \quad (3)
\end{aligned}
$$

There are six terms in expression (3). By scaling the six terms appropriately, equation (3) can become a better approximation to accurate delay data. The Fitted Elmore delay (FED) model is defined as follows.

$$
\begin{aligned}
&FED(r_d, c_l, l, w) \\
&= A \cdot r_d c_a l w + B \cdot r_d c_f l + C \cdot r_d c_l \\
&+ D \cdot \frac{r c_a l^2}{2} + E \cdot \frac{r c_f l^2}{2w} + F \cdot \frac{r l c_l}{w}
\end{aligned}
$$

where the coefficients A, B, C, D, E, and F are determined by a multiple linear regression [16] to accurate delay data.

The resulting model has several advantages over previous interconnect delay models:

1. FED is as efficient to compute as the Elmore delay model. Other accurate interconnect delay models are at least tens of times slower than our model.

2. As shown below, FED is significantly more accurate than Elmore delay and scaled Elmore delay models.

3. FED is written as a simple, explicit formula containing design parameters. This feature is very useful when designing interconnect optimization algorithms.

4. Because of its striking similarity to Elmore delay model, most previous interconnect optimization algorithms based on Elmore delay can use FED without much change.

To demonstrate the accuracy of the Fitted Elmore delay model, we test it on the $0.25\mu m$, $0.18\mu m$, $0.13\mu m$, and $0.07\mu m$ technologies described in [17]. The technology parameters are listed in Table 1.

Tech. (μm)	0.25	0.18	0.13	0.07
W_{min} (μm)	0.25	0.18	0.13	0.07
r_g (Ω)	16200	17100	22100	22100
c_g (fF)	0.282	0.234	0.135	0.066
r ($\Omega/\square$)	0.073	0.068	0.081	0.095
c_a ($fF/\mu m^2$)	0.059	0.060	0.046	0.056
c_f ($fF/\mu m$)	0.082	0.064	0.043	0.040

Table 1: Technology parameters.

Hspice is used to generate the accurate delay data. In the Hspice simulation, each wire is modeled as 30 π-type RC segments. The accuracy of our model is limited by the accuracy of Hspice data generated. So it is very important to generate accurate Hspice data. We are using the "ACCURATE" option and set the "MEASDGT" option to 10 in Hspice, which can make a 2-3% difference in the values generated.

To properly curve fit the Hspice delay data, we must generate an adequate number of data points in the region of interest for each technology. The region of interest and the number of values used for each design parameter are given in Table 2. We notice that just a few values for each design parameters are enough. For driver size, load size, and wire width, we are using 6 values uniformly distributed in the region of interest. However, for wire length, we observe that our model has a larger relative error when the wire is very short (i.e., the delay is very small). So 10 values are used for wire length and more values are chosen for small wire length. In addition, we start from $l = 450\mu m$ so that $l = 500\mu m$ will not be at the boundary of our model. In particular, we are using $l_i = 450 \cdot \gamma^{2^i - 1}$ where $i = 0, \ldots, 9$ and $\gamma = (18000/450)^{1/511}$. For each technology, we run Hspice on all combinations of design parameter values (i.e., $6 \times 6 \times 6 \times 10 = 2160$ points). The total CPU time for each technology is about 2 hours on a HP C360 machine with a 367 MHz processor and 512 MB of memory.

Design parameter	Region of interest	# points
Driver size (r_g/r_d)	$10\times$ to $510\times$ min. device	6
Load size (c_l/c_g)	$10\times$ to $510\times$ min. device	6
Wire width (w)	$1\times$ to $20\times$ W_{min}	6
Wire length (l)	500 to 18000 μm	10

Table 2: Region of interest and number of points used for design parameters.

The statistical package SAS [18] is used to perform a multiple linear regression on the Hspice data generated. The run time of SAS is negligible. The coefficients of the Fitted Elmore models for all technologies are given in Table 3. Since ED can easily overestimates delay by more than 30%, we use SED for comparison with FED. In order to make the relationship between FED and SED more apparent, the coefficients divided by $\ln 2$ are listed. Note that all the values in Table 3 are greater than 1. That means delay values by

SED is always smaller than those by FED. If wire resistance and capacitance dominate (i.e., terms associated with D and E are the most important), delay values by SED can be more than 10% smaller than those by FED.

Tech. (μm)	0.25	0.18	0.13	0.07
A / $\ln 2$	1.00724	1.00962	1.01258	1.01863
B / $\ln 2$	1.02993	1.03047	1.03010	1.02619
C / $\ln 2$	1.00332	1.00426	1.00511	1.00530
D / $\ln 2$	1.12520	1.12524	1.12673	1.13639
E / $\ln 2$	1.10598	1.10582	1.10463	1.09722
F / $\ln 2$	1.04665	1.04468	1.04836	1.06471

Table 3: Coefficients for the Fitted Elmore delay models.

Our model is now compared with SED for delay estimation. For each technology, delays by SED, FED, and Hspice are found for 3800 random points covering the whole region of interest. Then the absolute values of the relative error of SED and FED with respect to Hspice are calculated. The maximum and average error over the 3800 points are reported in Table 4. One can see that for our model, the maximum error is only 2% and the average error is less than 0.8%.

	Error in Delay			
	Maximum		Average	
Tech. (μm)	SED	FED	SED	FED
0.25	8.48%	1.68%	2.82%	0.69%
0.18	8.48%	1.79%	3.13%	0.73%
0.13	8.49%	1.94%	3.53%	0.79%
0.07	8.49%	2.00%	4.88%	0.73%

Table 4: Error in delay for scaled Elmore delay and our model.

Figure 1 shows the delay by Hspice, our model, and scaled Elmore delay model for $r_d = r_g/100$, $c_l = c_g \times 100$, $w = 6 \times W_{min}$ on 0.18 technology. Figure 2 shows an enlarged portion of Figure 1. Our model is virtually indistinguishable from the Hspice data.
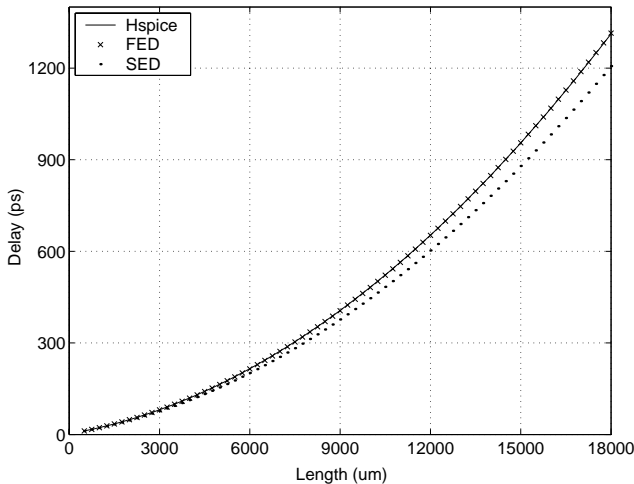

Figure 1: Delay comparison for one case on 0.18 technology.

We notice that our model is still very accurate for points outside of the region of interest. For each technology, we generate 500 random
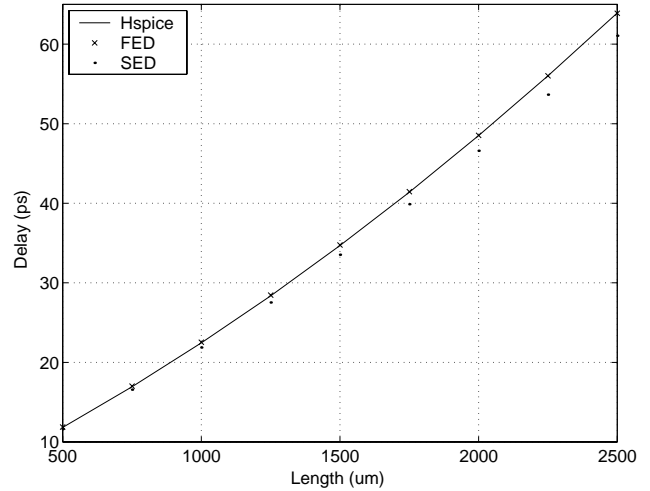

Figure 2: An enlarged portion of Figure 1.

points such that driver size and load size are from $5\times$ to $1020\times$ min. device, wire width is from $0.5\times$ to $40 \times W_{min}$, and wire length is from 500 to $36000\mu m$. The maximum and average errors in delay are reported in Table 5. There is no significant difference from the results in Table 4.

	Error in Delay			
	Maximum		Average	
Tech. (μm)	SED	FED	SED	FED
0.25	8.42%	1.57%	2.28%	0.69%
0.18	8.47%	1.91%	2.51%	0.80%
0.13	8.48%	1.92%	2.89%	0.90%
0.07	8.49%	2.41%	4.05%	0.99%

Table 5: Error in delay for points outside of the region of interest.

3. APPLICATION TO WIRE SIZING

In this section, we compare the accuracy of FED and SED when applied to sizing of uniform wires. We consider two wire sizing problems. The first problem is to optimize wire width to minimize delay. The second problem is to minimize wire width subject to delay bound. The delay bound is set to 10% over the optimal delay. All four technologies are tested. To fairly represent all possible design parameters, 100 random points in the region of interest are generated.

Note that to minimize delay, the optimal widths by SED and FED can be found by differentiating (1) and (2) with respect to w respectively.

$$\text{Optimal width by SED} \quad = \quad \sqrt{\frac{r(c_f l/2 + c_l)}{r_d c_a}}$$

$$\text{Optimal width by FED} \quad = \quad \sqrt{\frac{r(E c_f l/2 + F c_l)}{A r_d c_a}}$$

It is obvious that the minimize wire width subject to delay bound by SED and by FED can also be written in simple closed forms. To perform wire sizing in Hspice, a binary search is used to obtain the solutions.

The results on delay minimization are summarized in Table 6. The delay versus width for one of the random cases on the 0.18 technology is plotted in Figure 3. For this case, $r_d = r_g/13.59$, $c_l = c_g \times 121.40$, and $l = 2674\mu m$. This case generates an error of 6.16% for SED and an error of 2.47% for FED when compared with Hspice. This gives us a $2.5\times$ improvement over Elmore delay for this case. On average, for the 0.18 technology, our model produces a $3.4\times$ improvement.

| | Error in Wire Width | | | |
| | Maximum | | Average | |
Tech. (μm)	SED	FED	SED	FED
0.25	6.32%	2.44%	5.40%	1.55%
0.18	6.28%	2.62%	5.41%	1.61%
0.13	6.31%	2.68%	5.37%	1.68%
0.07	6.30%	2.97%	5.13%	1.81%

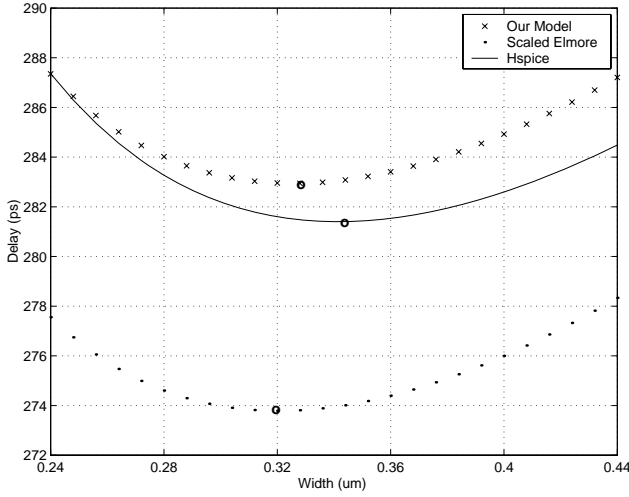**Table 6: Error in wire width for delay minimization.**

Figure 3: The delay versus wire width for one case on the 0.18 technology.

The results on wire width minimization subject to delay bound are summarized in Table 7.

| | Error in Wire Width | | | |
| | Maximum | | Average | |
Tech. (μm)	SED	FED	SED	FED
0.25	23.67%	2.40%	18.19%	1.32%
0.18	23.96%	2.67%	18.34%	1.34%
0.13	24.11%	2.85%	18.53%	1.28%
0.07	23.69%	4.28%	19.24%	0.83%

Table 7: Error in wire width for wire width minimization subject to delay bound.

SED performs poorly in this experiment. The average errors in wire width are more than 18%. In fact, because SED tends to underestimate the delay, all the wire widths computed according to SED are significantly less than those by Hspice. In other words, all the solutions by SED cannot satisfy the delay bound. If ED is used instead, since ED always significantly overestimates delay, there is no feasible solution (i.e., the delay bound is not achievable by ED) in

most cases. However, if a feasible solution is found, that solution is guaranteed to satisfy the delay bound. FED underestimates delay on about half of the cases. However, since FED is much more accurate, we observe that for all cases, FED solutions only violate the delay bound by much less than 0.1%.

4. EXTENSION TO INTERCONNECT TREE

In this section, we extend the Fitted Elmore delay model to handle an interconnect with tree topology. A simple tree as shown in Figure 4 is used to illustrate the idea.
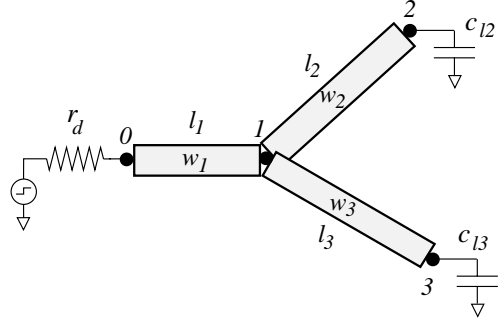

Figure 4: An example of a routing tree.

Elmore delay for node 2
$$
\begin{aligned}
=\ & r_d(c_a l_1 w_1 + c_f l_1 + c_a l_2 w_2 + c_f l_2 + c_a l_3 w_3 + c_f l_3 \\
& + c_{l2} + c_{l3}) \\
+\ & \frac{r l_1}{w_1}(\frac{c_a l_1 w_1 + c_f l_1}{2} + c_a l_2 w_2 + c_f l_2 + c_a l_3 w_3 + c_f l_3 \\
& + c_{l2} + c_{l3}) \\
+\ & \frac{r l_2}{w_2}(\frac{c_a l_2 w_2 + c_f l_2}{2} + c_{l2}) \\
=\ & r_d c_a(l_1 w_1 + l_2 w_2 + l_3 w_3) \\
+\ & r_d c_f(l_1 + l_2 + l_3) \\
+\ & r_d(c_{l2} + c_{l3}) \\
+\ & \frac{r c_a}{2}(l_1{}^2 + \frac{2 l_1 l_2 w_2}{w_1} + \frac{2 l_1 l_4 w_4}{w_1} + l_2{}^2) \\
+\ & \frac{r c_f}{2}(\frac{l_1^2}{w_1} + \frac{2 l_1 l_2}{w_1} + \frac{2 l_1 l_4}{w_1} + \frac{l_2^2}{w_2}) \\
+\ & r(\frac{l_1}{w_1}c_{l2} + \frac{l_1}{w_1}c_{l3} + \frac{l_2}{w_2}c_{l2})
\end{aligned}
$$

The Fitted Elmore delay model for interconnect trees is obtained by scaling the six terms above by the constants A, B, C, D, E, and F found by multiple linear regression for a single wire. There is no need to perform curve fitting again.

Fitted Elmore delay for node 2
$$
\begin{aligned}
=\ & A \cdot r_d c_a(l_1 w_1 + l_2 w_2 + l_3 w_3) \\
+\ & B \cdot r_d c_f(l_1 + l_2 + l_3) \\
+\ & C \cdot r_d(c_{l2} + c_{l3}) \\
+\ & D \cdot \frac{r c_a}{2}(l_1{}^2 + \frac{2 l_1 l_2 w_2}{w_1} + \frac{2 l_1 l_4 w_4}{w_1} + l_2{}^2) \\
+\ & E \cdot \frac{r c_f}{2}(\frac{l_1^2}{w_1} + \frac{2 l_1 l_2}{w_1} + \frac{2 l_1 l_4}{w_1} + \frac{l_2^2}{w_2}) \\
+\ & F \cdot r(\frac{l_1}{w_1}c_{l2} + \frac{l_1}{w_1}c_{l3} + \frac{l_2}{w_2}c_{l2})
\end{aligned}
$$

The idea above can be generalized to trees with any topology. For a general tree, let T be the set of indices of all tree edges. Let $T(i)$ be the set of indices of tree edges at the downstream of edge i. Let S be the set of indices of all sinks. Let $S(i)$ be the set of indices of sinks at the downstream of edge i. Let $P(k)$ be the set of indices of tree edges along the path from the driver to node k. Then

$$
\begin{aligned}
&\text{Fitted Elmore delay for node } k \\
&= \quad A \cdot r_d \sum_{i \in T} c_a l_i w_i \\
&+ \quad B \cdot r_d \sum_{i \in T} c_f l_i \\
&+ \quad C \cdot r_d \sum_{j \in S} c_{lj} \\
&+ \quad D \cdot \sum_{i \in P(k)} \frac{r l_i}{w_i} \left(\frac{c_a l_i w_i}{2} + \sum_{j \in T(i)} c_a l_j w_j \right) \\
&+ \quad E \cdot \sum_{i \in P(k)} \frac{r l_i}{w_i} \left(\frac{c_f l_i}{2} + \sum_{j \in T(i)} c_f l_j \right) \\
&+ \quad F \cdot \sum_{i \in P(k)} \frac{r l_i}{w_i} \left(\sum_{j \in S(i)} c_{lj} \right)
\end{aligned}
$$

Similar to Elmore delay, the Fitted Elmore delay for all nodes of an interconnect tree can also be calculated recursively in linear time.

To test the accuracy of our model, SED and FED of several trees with different number of sinks are calculated on the 0.18 technology. The error in delay with respect to Hspice simulation are reported in Figure 8. One can see that FED is again significantly better than SED. However, like the Elmore delay model, we observe that the accuracy of our model is adversely affected by the resistive shielding effect. This will be discussed in Section 6.

Tree	# sinks	Error in Delay			
		Maximum		Average	
		SED	FED	SED	FED
T1	2	3.06%	1.23%	2.34%	0.65%
T2	3	4.66%	0.32%	4.53%	0.17%
T3	4	9.36%	0.26%	9.32%	0.17%

Table 8: Error in delay for interconnect trees.

5. A MODEL HAVING THE SAME FORM AS ELMORE DELAY MODEL

Almost all previous algorithms and programs based on Elmore delay model can be used FED instead directly. However, for some results which depend heavily on the functional form of Elmore delay model (e.g., [19] [20]), it is not completely obvious whether FED can replace ED. It would be nice if there is a model with the same form as the Elmore delay model. In this section, we present such a model called *transformed Elmore Delay* (TED):

$$
\begin{aligned}
&TED(r_d, c_l, l, w) \\
&= \quad \alpha r_d (\hat{c}_a l w + \hat{c}_f l + \beta c_l) + \frac{\hat{r} l}{w} \left(\frac{\hat{c}_a l w}{2} + \frac{\hat{c}_f l}{2} + \beta c_l \right) \quad (4)
\end{aligned}
$$

This model is basically the same as the Elmore delay model as in (2). The only differences are the technology parameters are changed, and the driver resistance and load capacitance are scaled. As a result, all programs and algorithms based on the Elmore delay model

can be changed to use our model very easily and obtain much better results.

In order to obtain the coefficients α, β, $\hat{c}_a$, $\hat{c}_f$, and $\hat{r}$ so that TED is a good approximation of the Hspice data, we can equate the equations (1) and (4). So we want to have the following equalities.

$$
\begin{aligned}
\alpha \hat{c}_a &= A c_a \\
\alpha \hat{c}_f &= B c_f \\
\alpha \beta &= C \\
\hat{r} \hat{c}_a &= D r c_a \\
\hat{r} \hat{c}_f &= E r c_f \\
\hat{r} \beta &= F r
\end{aligned}
$$

By taking the logarithm of these six equalities, we have the following system of linear equations.

$$
M x = b
$$

where

$$
M = \begin{pmatrix} 1 & 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 \end{pmatrix}, \quad x = \begin{pmatrix} \log \alpha \\ \log \beta \\ \log \hat{r} \\ \log \hat{c}_a \\ \log \hat{c}_f \end{pmatrix}, \quad b = \begin{pmatrix} \log A c_a \\ \log B c_f \\ \log C \\ \log D r c_a \\ \log E r c_f \\ \log F r \end{pmatrix}.
$$

However, there are six equations but only five unknowns. So it is an overdetermined system. Thus we cannot expect to find an x that satisfies the system exactly. Instead we will seek an x which minimizes $\|Mx - b\|_2$. This is called the least-square problem and can be solved by QR factorization [21]. The parameters obtained by QR factorization for each technology are listed in Table 9. As before, in order to make the comparison with SED easier, $\alpha / \ln 2$ and $\hat{r} / \ln 2$ are listed. Notice that we can multiply α and $\hat{r}$ by a constant factor and divide β, $\hat{c}_a$, and $\hat{c}_f$ by the same factor without changing the delay value. We normalize the coefficients so that β is equal to 1.

Tech. (μm)	0.25	0.18	0.13	0.07
$\alpha / \ln 2$	0.98460	0.98765	0.98975	0.99505
β	1.00000	1.00000	1.00000	1.00000
$\hat{r} / \ln 2$	1.06378	1.06225	1.06464	1.07567
$\hat{c}_a$	1.03887	1.04061	1.04055	1.03994
$\hat{c}_f$	1.04150	1.04218	1.03917	1.02565

Table 9: Coefficients for the transformed Elmore delay models.

The error in delay for the transformed Elmore delay model is reported in Table 10. The maximum error of TED is only 0.8-0.89% worse than that of FED. On average, TED is only 0.13-0.55% worse than FED.

Tech. (μm)	Error in Delay	
	Maximum	Average
	TED	TED
0.25	2.51%	1.24%
0.18	2.68%	1.23%
0.13	2.79%	1.18%
0.07	2.80%	0.86%

Table 10: Error in delay for transformed Elmore delay model.

6. DISCUSSION AND FUTURE WORK

We observe that when FED is applied to interconnect trees, resistive shielding can cause it to overestimate the delay of sinks closer to the driver. We illustrate this point using the tree T1 in Table 8. Its topology is shown in Figure 4. For T1, $r_d = 500\Omega$, $l_1 = 1080\mu m$, $w_1 = 0.87\mu m$, $l_2 = 1120\mu m$, $w_2 = 0.31\mu m$, $l_3 = 810\mu m$, $w_3 = 0.31\mu m$, $c_{l2} = 62fF$, and $c_{l3} = 75fF$. The errors for sink 2 and sink 3 are 0.08% and 1.23% respectively. However, if we change w_2 to $0.09\mu m$ (i.e., half of the minimum width), our model will overestimate the delay for sink 2 and sink 3 by 5.48% and 7.51% respectively.

In the future, we would like to derive a model which takes resistive shielding into consideration. We would also like to incorporate inductive consideration into our model. The simple RLC delay model in [22] can be used instead of Elmore delay model. Another direction for future research is to include slope of input signal as a parameter.

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