Architecture Comparison for Concurrent Multi-Band Linear Power Amplifiers

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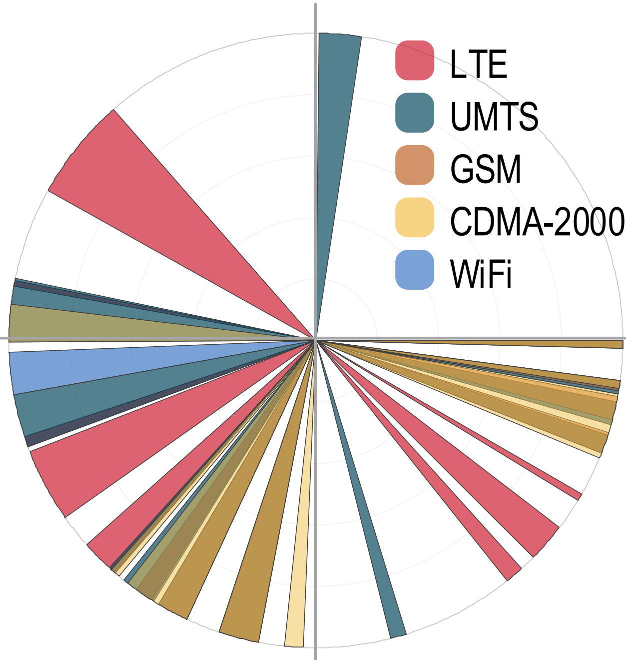
Outline

- Motivation
- Theoretical Comparisons
  - Efficiency
  - Linearity
  - Area
- Conclusions

Motivation

- Multiband radio is a basic requirement for today's wireless devices

- Current 4G standards propose carrier aggregation
  - Intra-band and inter-band
  - Contiguous and non-contiguous



Then

Now

Motivation

iPhone 5 mother board

PA Modules
Each IC contains several separate power amplifiers

- **Current approach consists of packing ever more separate PAs into a device**
  - Large area
  - Complex signal routing
  - Complex control

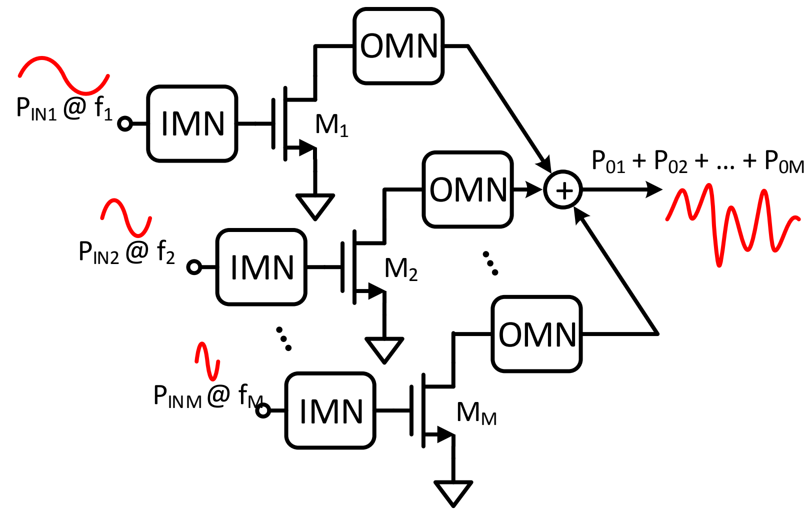
- **Such architectures do not inherently support simultaneous multi-band signals**

- **In light of this, researchers are now beginning to develop simultaneous multi-band PA architectures**

Motivation

- There are two primary approaches for realizing concurrent multi-band PAs

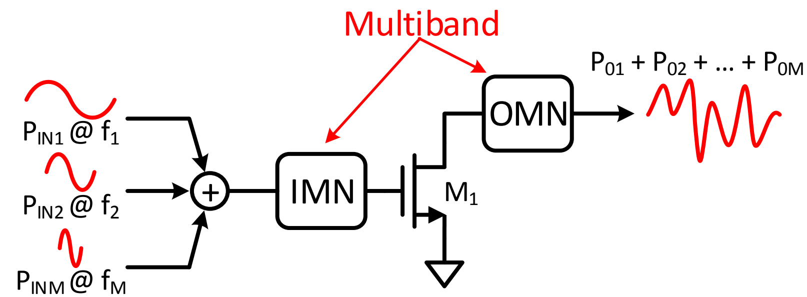
Parallel Single-Band



- Multiple parallel single-band PAs
  - Larger area
  - Must have some way of combining the output signals

- Single multi-band PA
  - Fewer components
  - Theoretical drop in efficiency

Concurrent Multi-Band



- Which approach is "better"?

Efficiency Comparison

- **Drain efficiency is defined as:**

$$\eta = \frac{P_L}{P_{DC}}$$

P_L – Power delivered to the load
P_{DC} – Power consumed from the DC supply

- **Multi-band output power is defined to be the total power in ALL DESIRED bands**

$$P_L = P_{f1} + P_{f2}$$

- **Assuming a linear device and 2 bands, the drain current is:**

Single Stage in Parallel Single-Band

$$I_{D,PS} = I_{DC,M} + \underbrace{i_{rf,M}\cos(2\pi f_M t + \theta_M)}_{\text{Load Current of single stage}}$$

Concurrent Multiband

$$I_{D,MB} = I_{DC} + \underbrace{i_{rf}\cos(2\pi f_1 t) + i_{rf}\cos(2\pi f_2 t + \theta)}_{\text{Load Current}}$$

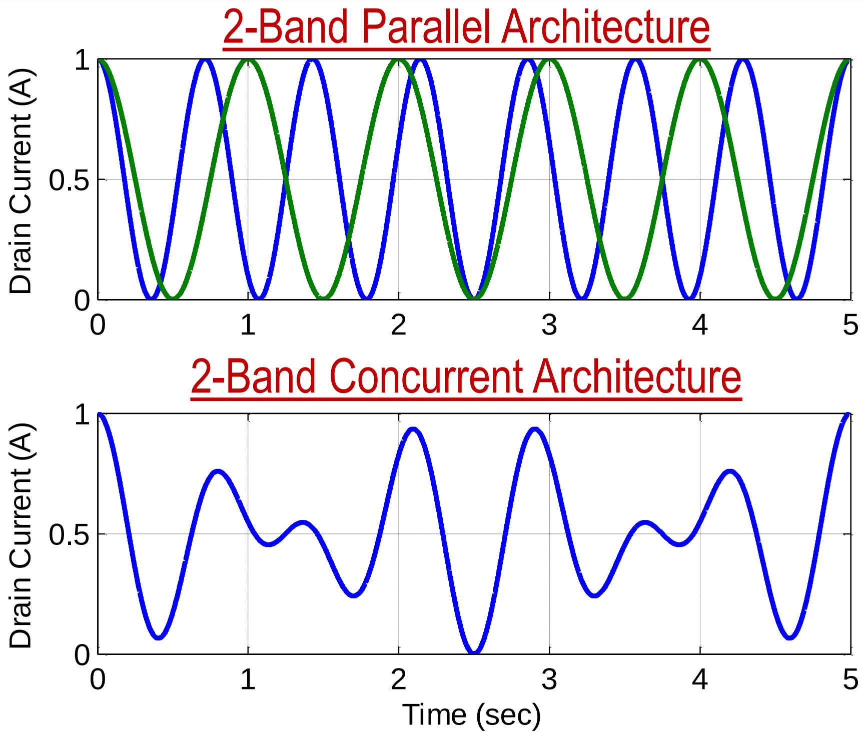
Efficiency Comparison

- **The drain current swing is fixed such that $0 \le I_D \le 1$**

- **Parallel, single-band architecture**
  - Class A: $i_{rf,M}$ = 0.5 and I_{DC} = 0.5
  - Class B: $i_{rf,M}$ = 1 and I_{DC} = 0
  - Class C: $i_{rf,M}$ = 1.25 and I_{DC} = -0.25

- **Single, multi-band architecture**
  - Numerical methods are used to set i_{rf} and I_{DC} for each class of operation

- **Sweep f_2/f_1 from 1 to 10**



	Parallel Single-band	Single Multi-band
Class-A	50 %	25 %
Class-B	78.5 %	62 %
Class-C	82 %	71 %

Efficiency Comparison

- **Efficiency can be increased by slightly overdriving the amplifier**
  - Non-linear model presented in RF Power Amplifiers for Wireless Communication by S. Cripps is used for this investigation

$$I_D(t) = 3V_G^2(t) - 2V_G^3(t)$$

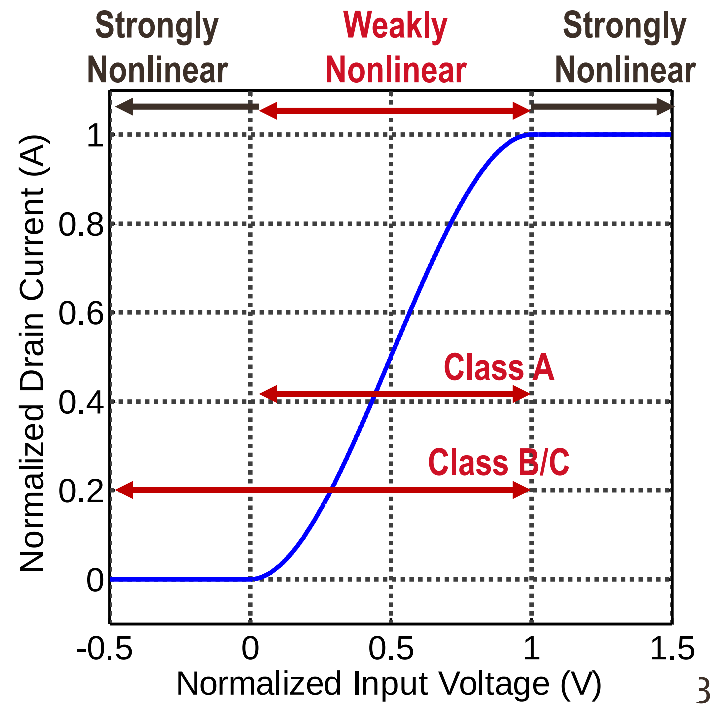
- **Parallel, single-band architecture**

$$V_G(t) = V_{DC} + v_{rf}cos(2\pi f_M t + \theta_M)$$

- **Single, multi-band architecture**

$$V_G(t) = V_{DC} + v_{rf}cos(2\pi f_1 t) + v_{rf}cos(2\pi f_2 t + \theta)$$

- **v_{rf} and V_{DC} are set such that $0 \le V_G(t) \le 1$**

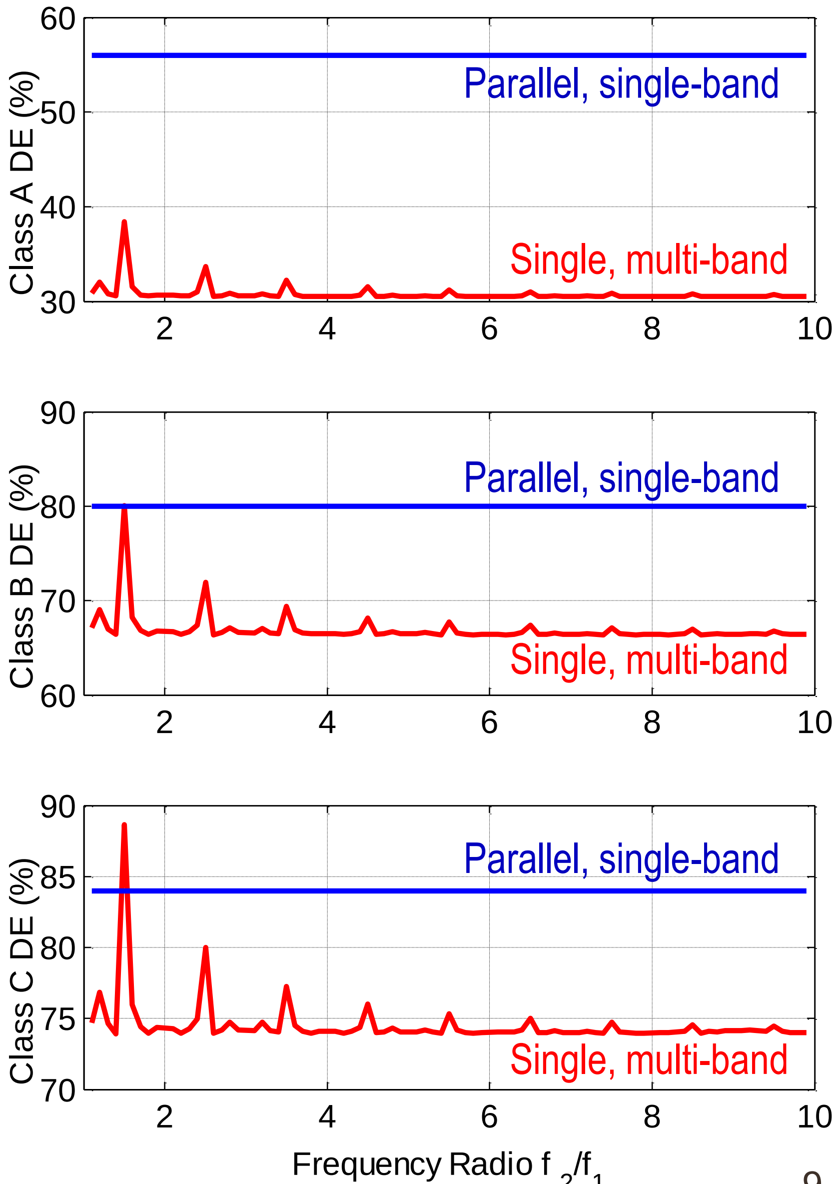


Efficiency Comparison

- **Compressed drain efficiency for parallel single-band power amplifier**
  - Class-A: $\eta_{ave} = 56\%$
  - Class-B: $\eta_{ave} = 80\%$
  - Class-C: $\eta_{ave} = 84\%$

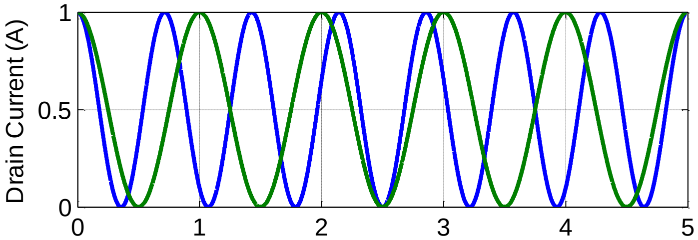
- **Compressed drain efficiency for single multi-band power amplifier**
  - Class-A: $\eta_{ave} = 31\%$
  - Class-B: $\eta_{ave} = 67\%$
  - Class-C: $\eta_{ave} = 75\%$

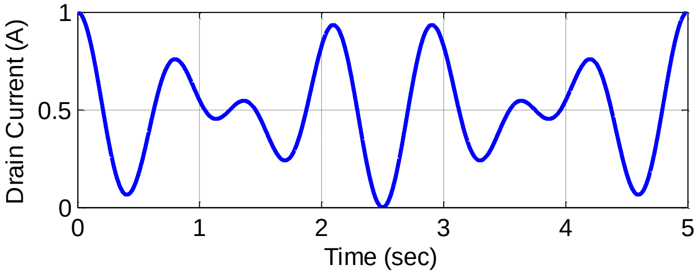
- **Outputs are ideally filtered to remove all non-linear distortion at the LOAD**

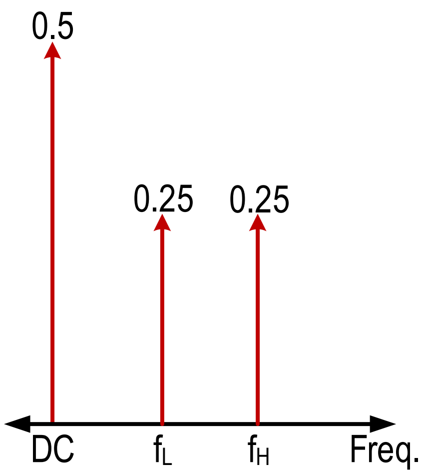


Efficiency Comparison

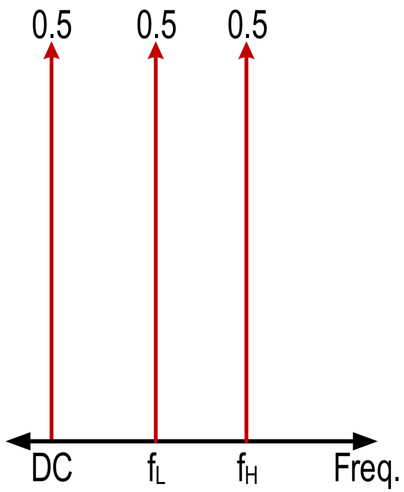
- **There is a significant drop in efficiency in the single, multi-band architecture**
  - Class-A: Reduction of 25%
  - Class-B: Reduction of 13%
  - Class-C: Reduction of 9 %
- **This is due to the reduced power in each band**
  - This is improved by overdriving the amplifier
- **Variation in efficiency as a function of frequency ratio can be predicted by the peak-to-average-ratio of the input**
  - Lower PAR leads to higher drain efficiency







Single, multi-band



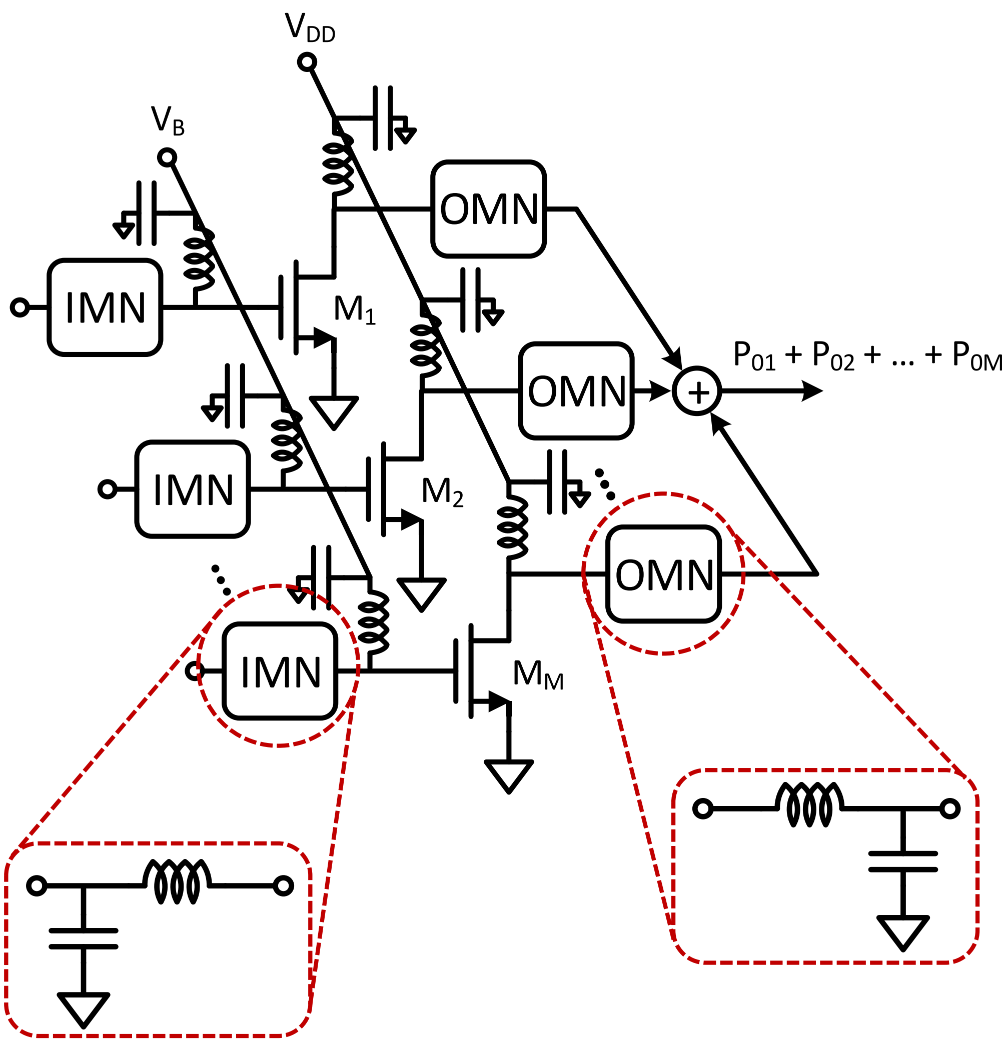
Parallel, single-band

Linearity Comparison

- **Linearity is especially critical in concurrent multi-band systems**
- **Parallel, single-band architecture**
  - Nonlinear distortion causes harmonic generation only
  - Linearity of diplexer may be an issue
  - No limitations on frequency separation
- **Single, multi-band architecture**
  - Nonlinear distortion causes harmonic AND intermodulation components
  - Restrictions on frequency choices
    - Becomes much more complicated for larger number of bands
- **Both cases will require good filtering at the output**
  - Filtering in the parallel, single-band case will depend on the diplexer

Area Comparison

◆ Component count can be a good indication of board area



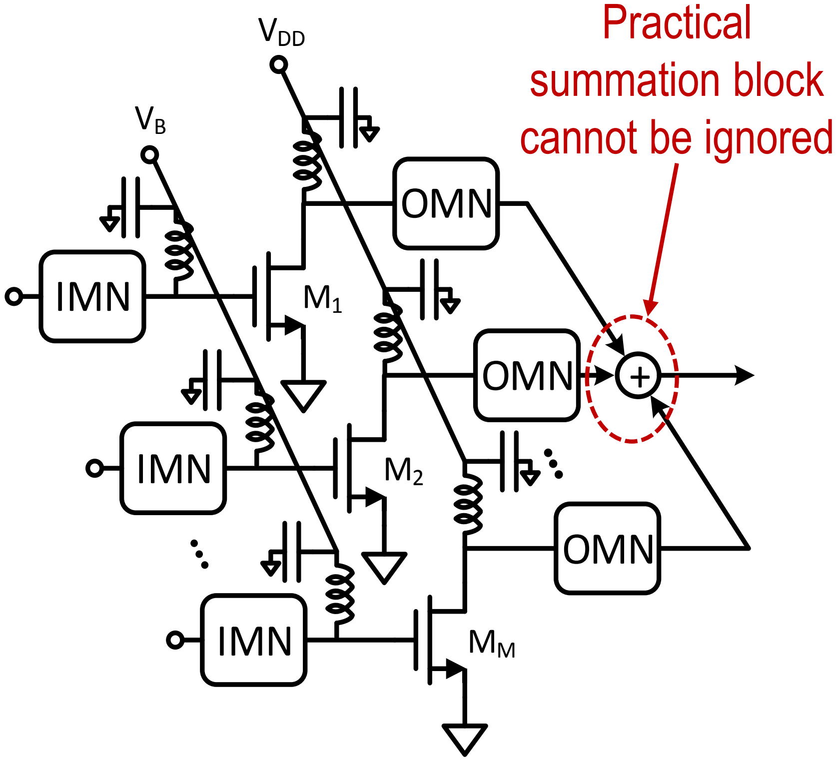
Component Count for Parallel Single-band Architecture

	Component Count
Input L-Match	2M
Output L-Match	2M
RF Chock	2M
RF Bypass	2M
Power Transistor	M
Power Combiner	1
Total	9M+1

*M is the number of supported bands

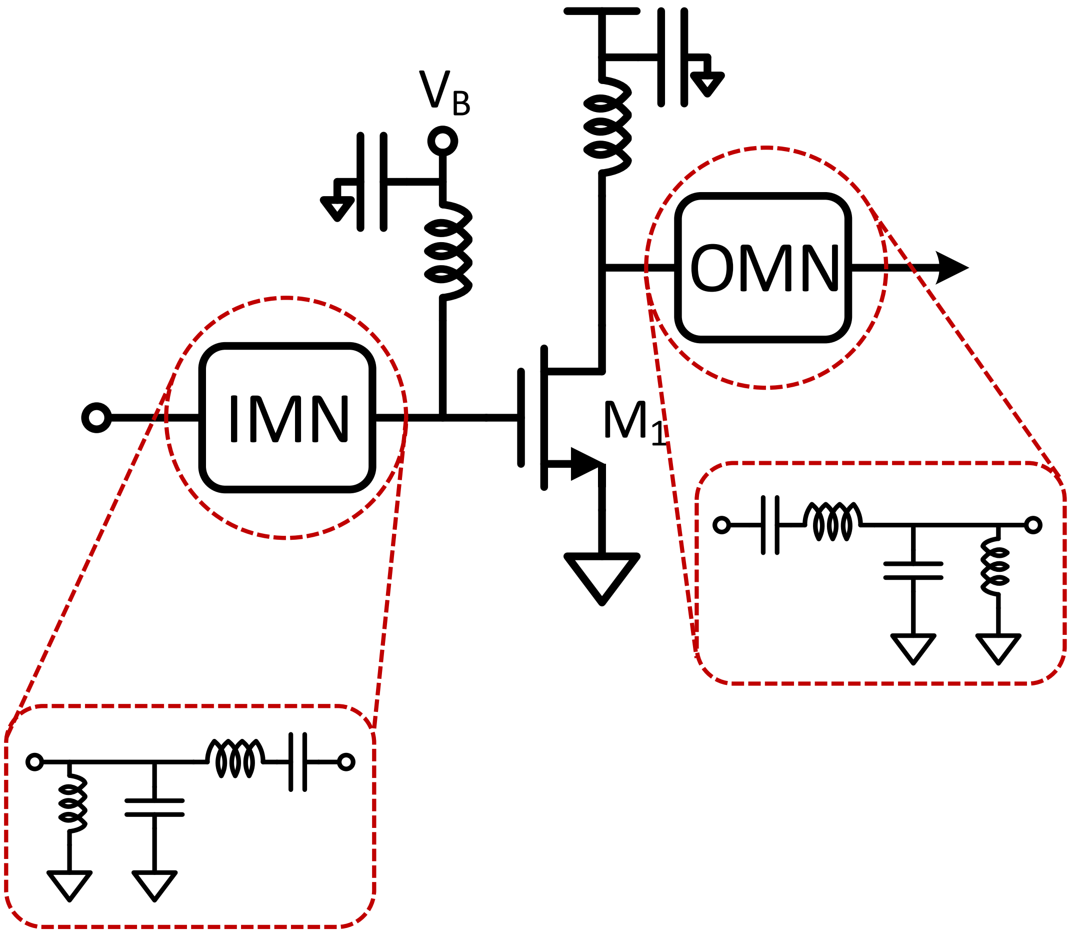
Area Comparison

- **To now we have assumed ideal summation of the output signals**
  - Practical implementations will use diplexer



	Ref.	Insertion Loss	Area
2-bands	TDK 202690DT	~0.4 dB	2×1.3 mm^2
	TDK 105950DT	~0.5 dB	1×0.5 mm^2
	Zou et al., MWCL 2012	~0.5 dB	14×8.2 mm^2
3-bands	Dai et al., ICMMT 2012	~0.5 dB	3×4 mm^2
	Chongcheawchamnan et al., MWCL 2006	~3.4 dB	55×31 mm^2
	Hayati et al., TMTT 2013	~3.5 dB	90×90 mm^2

Area Comparison



Component Count for Single, Multi-band Architecture

	Component Count
Input L-Match	2M
Output L-Match	2M
RF Chock	2
RF Bypass	2
Power Transistor	1
Power Combiner	N/A
Total	4M+5

*M is the number of supported bands

Area Comparison

- **Area is further compared using an example implementation**
  - Assume a lumped-element implementation of both architectures
  - Assume dual-band support
  - 20% added to account for routing

Component	Area/ (Technology)	Parallel Single-Band		Single Multi-Band	
		Num. of Components	Area	Num. of Components	Area
Inductor/Capacitor (Matching Network)	0.125 mm^2/ (0201)	8	1 mm^2	8	1 mm^2
RF Choke Inductor	0.5 mm^2/(0402)	4	2 mm^2	2	1 mm^2
RF Bypass Capacitor	31 mm^2/(2917)	4	124 mm^2	2	62 mm^2
Power Transistor	36 mm^2/ Cree GaN FET	2	72 mm^2	1	36 mm^2
Diplexer	40 mm^2/Ave. 2-band diplexers	1	40 mm^2	0	
Total		**19**	**286 mm^2**	**13**	**120 mm^2**

Conclusions

- **Two popular power amplifier architectures for supporting concurrent multi-band signaling have been compared**

- **Efficiency**
  - Parallel, single-band architecture
    - Much higher efficiency for class-A
    - Gap is reduced for class-B and –C
    - Additional reduction in efficiency due to diplexer
  - Single, multi-band architecture
    - Reduced output power, per band, for the same DC bias
    - Efficiency depends upon frequency ratio as well as initial phase offset

- **Linearity**
  - Parallel, single-band architecture
    - Essentially the same linearity requirements as traditional single-band amplifiers
  - Single, multi-band architecture
    - Significant harmonic and inter-modulation distortion
    - Limits the choice of frequency bands
    - Becomes more severe as the number of supported bands increases

Conclusions

- **Area**
  - Parallel, single-band architecture
    - Requires significantly more components
    - Diplexer
  - Single, multi-band architecture
    - Requires only a single set of RF choke and RF bypass devices

- **The need for a diplexer will be the limiting factor for the parallel, single-band architecture**
  - Large – Ranging from 0.5 to 115 mm^2 for dual band and 12 to 8100 mm^2 for triple band
  - Lossy – Triple-band diplexers have insertion losses of several dB
  - Expensive – Commercial examples cost in the dollar range
  - Unclear how more than three bands can be supported

Acknowledgements

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Thank You